A Digitally Tunable Analogue Conditioning Circuit for Angular Position Sensors

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***Abstract*—This paper shows a digitally tunable analogue processing architecture based on an adaptive circuit. The conditioning circuit has been designed to extend the linear range of an angular position sensor, compensating the output drift due to temperature variations. System-level simulations give a temperature-independent linear output in the range of 293-353 K, with an accuracy of 2 degrees in the angular position. Inherent low power and low size characteristics make these circuits valuable to implementing the "smartness" part of smart sensors.**

I. INTRODUCTION

Sensors are the front-end of processing devices connected to real-world systems. Most of sensors present a limited linear range, reducing the effective application span. Using electronic circuits to sensor behavior pre-processing extends its available working range. Adaptive circuits based on artificial neural networks makes possible to modify the compensation circuit behavior, tuning its parameters according to new requirements. Thus, selecting a set of suitable parameters, an adaptive electronic circuit will improve the operation of a sensor, extending its linear response independently of temperature drifts.

Giant magneto-resistive sensors (GMR) [1] are devices which resistance depends on its position within a magnetic field. GMR sensors are useful in angular position detection. However, GMR behavior is linear in only a limited range (Fig. 1). When a wider linear range is required, a conditioning circuit must be incorporated.

Adaptive computing tools based on the operation of biological neurons [2] consist of a set of processors, highly interconnected and arranged in layers. System operation is tuned using a training process where input-output samples from the desired task are iteratively presented, adjusting the network weights that connect inputs from a neuron layer to the preceding neuron layer outputs. When size, power consumption and speed are main requirements, electronic analogue implementation is a suitable selection [3] [4] [5]. Moreover, current-mode analogue circuits give better results at lower bias, reducing the power consumption [6]. In these cases, implementation of reliable long-term and mid-term weights using digital registers as storage elements, combined with analogue processing electronics can improve considerably the system features [7] [8].

This paper shows a digitally tunable current-based adaptive processing circuit designed to extending the linear range of a GMR sensor, compensating the output drift caused by working temperature changes in a 60 K span. Expected minimum angular position accuracy is 2 degrees.

Section II shows the processor architecture, circuit schematics and transistor dimensions. System-level model, conditioning architecture and parameter fitting process are described in Section III. Following, in Section IV the proposed system-level model is applied to improve the characteristic of a GMR, showing partial results and final output, comparing to the original sensor behavior.

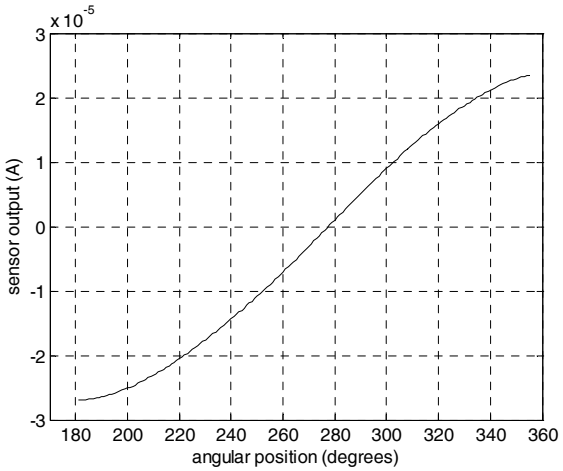

Figure 1. Giant magneto-resistive sensor behavior

This work has been supported by DGA-FSE (T51/2005), MCYT-FEDER (TIC2002-00636) and Univ. of Zaragoza (UZ2002-TEC-05)

II. PROCESSING UNIT

Processing electronics is based on a current-mode circuit designed using the Austria Microsystems 0.35µm design kit. Fig. 2a shows the block diagram of the adaptive processor used in this work. Processor consists of a current-based mixed analogue-digital multiplier and a current conveyor that executes the non-linear processor operation.

A. Multiplier Circuit

The proposed analogue-digital multipliers (ADM in Fig. 2) [7] [8] multiply the analogue current inputs (i_i) by the 8-bit digital word $\bar{b}_i$ that represents the tunable network weights. This circuit contains a current inverter controlled by the sign bit of the digital operand plus a 7-bit digitally programmable current divider. Current output ranges from I_{in} to $-I_{in}$ (maximum and minimum input currents respectively). An analogue multiplexer selects the current input path to the R-2R transistor-based ladder. When weight sign bit is positive (b_0=0 v), current goes to the divider straight; if sign bit is negative (b_0=3.3 v), current is driven to the inverter, changing the sign of the output current.

1) Programmable current divider. The main four-quadrant multiplier building block consists of an R-2R ladder circuit implemented with NMOS transistors. This structure (Fig. 3), widely presented in the literature [9] [10] [11], allows the current to flow in both directions and is designed using identical 0.3 µm length and 10 µm width transistors working in triode mode.

Gate voltages b_i (Fig. 3) control the current flow to the right-side transistors (b_i =0 v) or the left-side transistor (b_i =3.3 v). For N bits, output currents are described according to

$$I_{out_1} = I_0\left(\sum_{n=1}^{N}\frac{b_n}{2^n}\right) \quad (1)$$

$$I_{out_2} = I_0\left(\frac{1}{2^N}+\sum_{n=1}^{N}\frac{\bar{b}_n}{2^n}\right) \quad (2)$$

where I_{out1} and I_{out2} are the lower and upper output currents. In our work, I_{out1} has been selected as the final output current. Thus, according to (1), digital weight absolute value ranges from 0 to $1-1/2^N$. Assuming a 7 bits plus sign weight representation, digital operand minimum module value equals to $7.8125\cdot10^{-3}$.

2) Current inverter. Multiplier sign bit is implemented using a class AB current follower (Fig. 4). This structure gives a centered low-distortion current using a ± 2 v bias voltage. Tables 1 and 2 show the current follower design characteristics and transistor sizes, respectively. The bias current value (30 µA, see Table 1) ensures a very low distortion in the processing signals range.

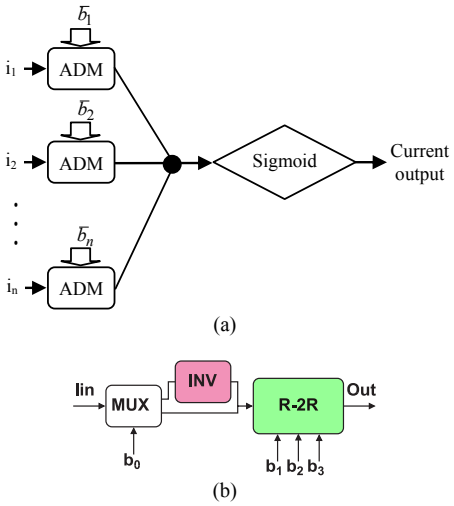

Figure 2. Neuroprocessor architecture. (a) main building blocks; (b) Analogue-digital multiplier architecture

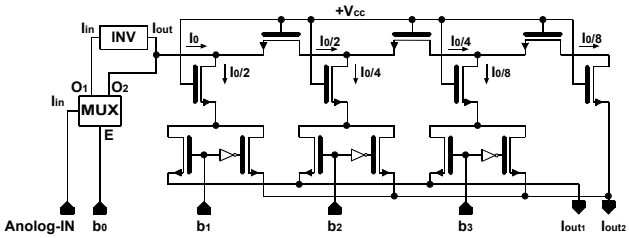

Figure 3. Current-based analogue-digital multiplier circuit

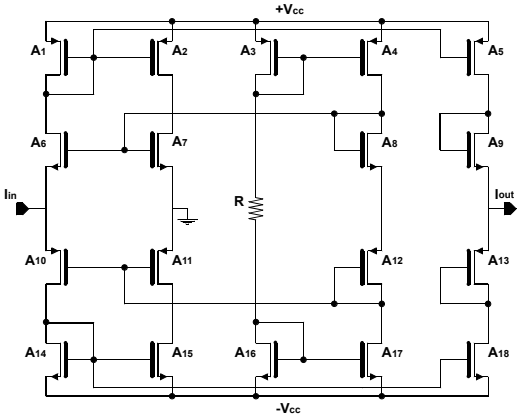

Figure 4. Current follower

B. Activation Function

Activation function circuit consists of a class AB current conveyor (Fig. 5), similar to the circuit proposed in [7]. Circuit output has hyperbolic tangent type behavior. Design characteristics and transistor dimensions are shown in Tables 3 and 4 respectively.

TABLE I. CURRENT FOLLOWER DESIGN CHARACTERISTICS

PARAMETER	VALUE
$\pm V_{cc}$ [V]	±2
I_{bias} [µA]	30
Vgs [V]	±1
Vds [V]	±1

TABLE II. CURRENT FOLLOWER TRANSISTORS DIMENSIONS

Transistors	W [µm]	L [µm]
A_1,A_2,A_3,A_4,A_5	4.25	0.3
A_6,A_7,A_8,A_9	13.00	0.3
A_{10},A_{11},A_{12},A_{13}	48.15	0.3
A_{14},A_{15},A_{16},A_{17},A_{18}	0.85	0.3

TABLE III. ACTIVATION FUNCTION DESIGN CHARACTERISTICS

PARAMETER	VALUE
$\pm V_{cc}$ [V]	±2
I_a [µA]	5
I_b [µA]	50
V_{gs} [V]	±1
V_{ds} [V]	±1

TABLE IV. ACTIVATION FUNCTION TRANSISTORS DIMENSIONS

Transistors	W [µm]	L [µm]
B_1, B_2, B_3	0.90	0.3
B_4	5.35	0.3
B_5, B_6, B_7	6.90	0.3
B_8, B_9	1.90	0.3
B_{10}	2.85	0.3
B_{11}	0.65	0.3
B_{12}, B_{13}	8.70	0.3
B_{14}	0.70	0.3
B_{15}	0.60	2.1
B_{16}, B_{17}, B_{18}	0.60	1.7
B_{19}	1.20	0.3
B_{20}, B_{21}, B_{22}	1.40	0.3

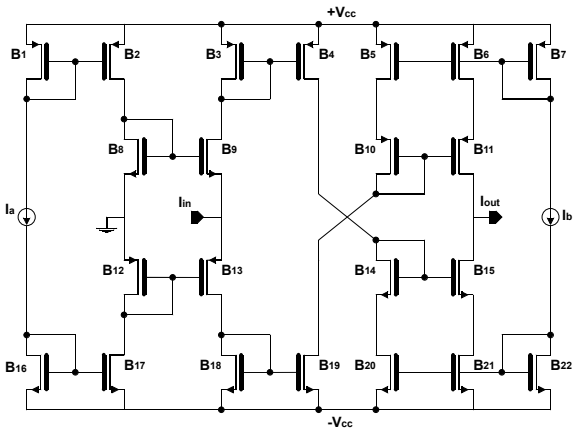

Figure 5. Current-based hyperbolic tangent function

III. SYSTEM ARCHITECTURE

Processing elements was simulated using Spectre Simulator, from Cadence Design Framework. Achieved results have been used to develop the system-level models applied in the GMR characteristic conditioning example.

A. System-Level Models

Four-quadrant mixed-mode multiplier behavior has been numerically modeled using Matlab. In our design, multiplier operation can be realistically expressed by:

$$out = 0.974865wp - 0.0136726p \quad (3)$$

Where w is the digital operand and p is the analogue input. Once input currents are weighted and accumulated, final output is carried out by means of a current conveyor (Fig. 5) [12], which performs the non-linear neuron operation. In order to achieve a valuable accuracy in system simulations, current conveyor operation is simulated using a look-up table. Differences between simulated circuit operation and ideal hyperbolic function are described as a relative error:

$$R_{err} = 100 * (F' - F)/F \quad (4)$$

Where F' is the simulated realistic non-linear output function and F is the ideal hyperbolic tangent function. Relative error as a function of input current is presented in Fig. 6.

B. Temperature Compensation Unit

Our goal is to apply the proposed tunable processing circuit to improve the characteristic of an angular position sensor, extending the linear output range and reducing the output drift due to temperature changes. Many sensors present an output drift due to changes in temperature operation. Fig. 7 shows the behavior of a GMR at four different temperatures. A conditioning system must compensate this output drift, giving the same sensor behavior independent of temperature.

The proposed temperature-compensation circuit is presented in Fig. 8. A multilayer perceptron (MLP) [2] receives the actual temperature (from a linear diode-based temperature sensor) and sensor output as inputs, correcting the output drift and giving the expected sensor measure at a determined temperature as output. Hidden nodes architecture is as presented in Fig. 2, whereas the output node function is linear (current goes out directly from the multiplier unit).

Network weights are tuned using a training process based on the classical perturbative learning algorithm proposed in [13]. The use of this algorithm is due to its robustness to neuron non-idealities compared to gradient descent-based techniques [3]. Basically, a weight perturbative algorithm slightly changes the value of a selected weight w_p adding and subtracting the perturbation (*pert*), evaluating the root mean square error achieved in the conditioning transfer function in both cases:

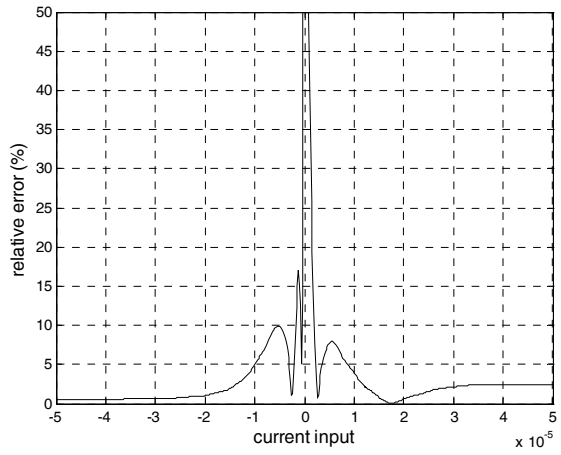

Figure 6. Real tanh function relative error

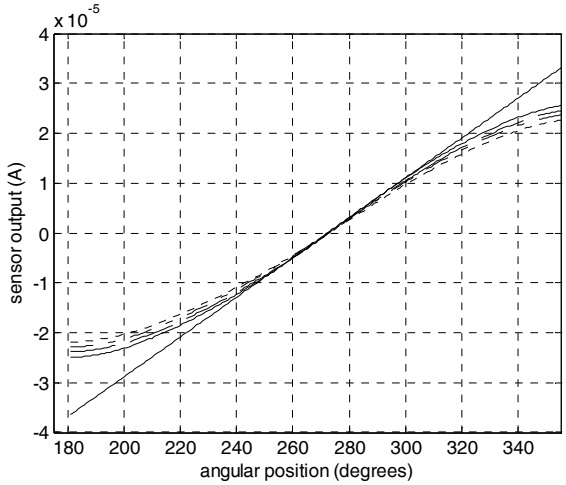

Figure 7. GMR sensor output at 293 K (solid line), 313 K (dashed line), 333 K (dash-dot line) and 353 K (dotted line)

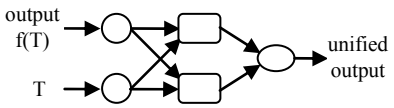

Figure 8. Temperature compensation network

$$w'_p = w_p + pert;\ E_1 = rms(\sum_i (o_i - f(w'_p)) \qquad (5)$$

$$w''_p = w_p - pert;\ E_2 = rms(\sum_i (o_i - f(w''_p)) \qquad (6)$$

In (5) and (6), o_i are the desired network output for each input pattern i, and $f(w_p)$ the neural network transfer function. Thus, E_1 and E_2 are the whole achieved root mean square errors when the perturbation is added and subtracted, respectively.

Finally, the weight is modified according to

$$w(t+1) = w(t) + \xi(E_2 - E_1)/pert \qquad (7)$$

where ξ is a value lower than 1. Thus, in the next iteration (t+1), a new weight is selected and the process is go over, until the system reaches the expected maximum error.

C. *Output Linearization*

Once temperature drift is compensated, a neural linearization circuit based on [8] (Fig. 9) gives the final linear output. The proposed MLP has a hidden layer with four processing elements, whose block diagram was presented in Fig. 2. As in the case of the temperature compensation circuit, training process is based on the perturbative algorithm.

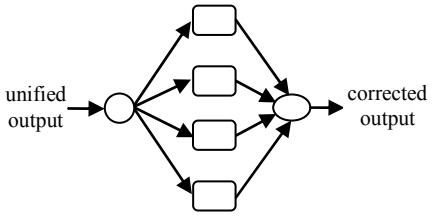

Figure 9. Sensor output linearization system

IV. APPLICATION TO GMR SENSORS

GMR output temperature dependence (Fig. 7) is corrected using the neural network architecture presented in Fig. 8. Temperature-compensation circuit is trained in order to provide the sensor response at 293 K, independently of the actual working temperature in the 60 K degrees range from 293-353 K. Fig. 10 shows the resulting compensated sensor outputs. As we can see, differences in the sensor output, working at the proposed 60 K degrees span are drastically reduced.

Fig. 11 shows the final corrected sensor output working at 293, 313, 333 and 353 K degrees. In this application, the expected (ideal) linear output used in the training phase is tangent to the linear characteristic of the sensor at 293 K, in the middle of the output range (Fig. 10). As we can see in this figure, resulting outputs are closer to the ideal output than the actual sensor output at 293 K degrees, represented in the figure with a dash-dot line.

The goal of this work is to linearize the GMR sensor behavior, giving the angular position with an error lower than 2 degrees, independently of the temperature. Differences between the ideal expected behavior and the temperature-free linearized sensor characteristic are presented in Fig. 12 and compared to the actual sensor error at 293 K degrees.

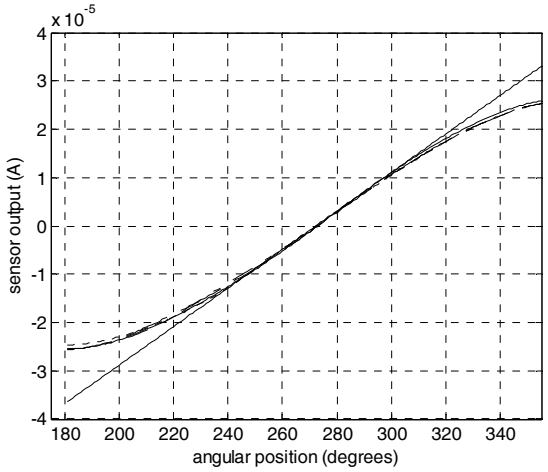

Figure 10. Temperature compensated sensor outputs

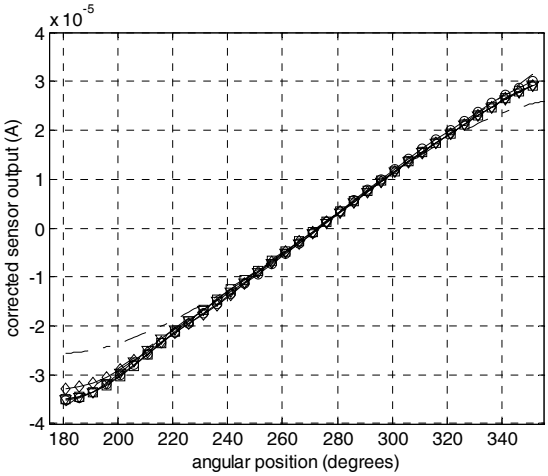

Figure 11. Linearized sensor outputs for a sensor at 293 (circles), 313 (triangles), 333 (squares), and 353 (diamonds) kelvin degrees, compared to the actual sensor output at 293 K degrees (dash-dot line)

V. CONCLUSIONS

This work presents simulation results of a mixed analogue-digital system designed to conditioning GMR sensors behavior, compensating the output drift due to changes in working temperature and extending the linear output span. System consists of two stages. In the first one, temperature drifts are corrected, giving an output similar to the sensor response at 293 K. The second stage extends the linear range of the sensor at this temperature, assuming a maximum error of 2 degrees in the measured angular position. Table V shows the linear ranges achieved using the compensation system: The global system improvement is higher than 70%, compared to the linear range of the non-corrected sensor output at the reference temperature (293 K).

According to the table values, it seems possible a wider extended linear range, selecting a more suitable linear output target.

On the other hand, digital weight storage allows an easy system tunability. Thus, it is possible to modify the processing system operation according to changes in the sensor behavior due to aging or variations in the working conditions, extending the sensor life.

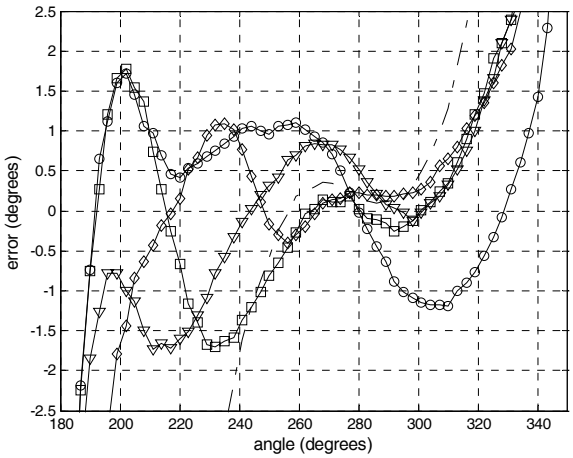

Figure 12. Corrected sensor output errors compared to the ideal linear response. Markers are as in Fig. 11

TABLE V. EXTENDED LINEAR RANGE

Temperature (K)	Extended range (err<2 deg.)	Improvement
293	188-342	105%
313	189-327	84%
333	188-327	84%
353	198-329	75%
Global behaviour	**198-327**	**72%**
Sensor behaviour	**239-314**	

REFERENCES

[1] J. G. Webster, The Measurement, Instrumentation and Sensors Handbook. IEEE Press, 1999.

[2] S. Haykin. Neural Networks, a Comprehensive Foundation. Prentice Hall, 1999.

[3] M. Valle, "Analog VLSI implementation of artificial neural networks with Supervised On-Chip Learning", Analog Integrated Circuits and Signal Processing, vol. 33 pp. 263-287, 2002.

[4] M. Jabri, R. J. Coggins, B. G. Flower, Adaptive Analog VLSI Neural Systems, Chapman & Hall, June 1990.

[5] M. Milev, M. Hristov, "Analog Implementation of ANN with Inherent Quadratic Nonlinearity of the Synapses", IEEE Trans. on Neural Networks, 2002, vol. 14, n. 5, pp. 1187-1200.

[6] C. Toumazou, F. J. Lidgey, D. G. Haigh, "Analogue IC Design: The Current-Mode Approach", IEE Circuits and Systems Series 2. 1990.

[7] C. Lajusticia, N. Medrano, G. Zatorre, B. Martin, "Applying Non-Ideal Mixed Analog-Digital Multipliers in Electronic Processing Circuits Based on Neural Networks", Proc. 2003 IEEE Conference on Emerging Technologies and Factory Automation, ETFA 2003, vol. 2, pp. 362-367.

[8] G. Zatorre, N. Medrano, S. Celma, "A mixed-mode artificial neural network model applied to sensor output improvement". Proc. 11th Intl. Conf. on Mixed Design of Integrated Circuits and Systems MIXDES 2004, pp. 134-139.

[9] K. Bult, G. Geelen, “An Inherently Linear and Compact MOST-only Current Division Technique”, IEEE J. Solid-State Circuits 1992, vol. 27, n. 12, pp 1730-1735.

[10] B. Linares-Barranco, T. Serrano-Gotarredona, R. Serrano-Gotarredona, “Compact Low-Power Calibration Mini-DACs for Neural Arrays With Programmable Weights”, IEEE Trans. on Neural Networks, vol. 14, no. 5, pp. 1207-1216, Sept. 2003.

[11] M. T. Sanz, B. Calvo, S. Celma, C. Morán, “A Digitally Programmable VGA”, IEEE Midwest Symposium on Circuits and Systems, MWSCAS 2001, pp. 602-605.

[12] K. Wawryn and A. Mazurek, “Prototype Circuits for Programmable Neural Network”, European Conference on Circuits Theory and Design, ECCTD 2001, vol. 3, pp. III-301 - III-304.

[13] M. Jabri, B. Flower, “Weight perturbation: An optimal architecture and learning technique for analog VLSI feedforward and recurrent multilayer networks”, IEEE Transactions on Neural Networks, vol. 3 no. 1 pp. 154-157, January 1992.